239. The system of claim 238 in which the stack-based instructions are Java bytecodes.

240. The system of claim 239 wherein the certain instructions include Java bytecodes for method invocations.

241. The system of claim 238 in which the translation software is part of a virtual machine.

242. The system of claim 241 in which the virtual machine is a Java virtual machine.

243. The system of claim 238 wherein the first unit and the hardware unit are part of a central processing unit.

244. The system of claim 238 wherein the first unit comprises a central processing unit and the hardware unit is outside of the central processing unit.

245. The system of claim 238 wherein a portion of the operand stack is stored in a register file of the first unit, the hardware unit is adapted to produce at least one overflow/underflow indication for the portion of the operand stack stored on the register file.

246. The system of claim 238 wherein the hardware unit is connected between a memory and the first unit.

247. The system of claim 238 wherein the hardware unit is adapted to examine the stack-based instructions to determine whether multiple stack-based instructions can be combined into fewer register-based instructions.

248. The system of claim 247 wherein the hardware unit produces register-based instructions that access the portion of the operand stack in the register file so as to reduce the number of register-based instructions that would otherwise be required.

249. A system comprising:

a first unit adapted to execute register-based instructions; and

a hardware unit associated with the first unit, the hardware unit adapted to convert Java bytecodes into register-based instructions, wherein certain Java bytecodes are not translated in the hardware unit but instead cause a modified Java Virtual machine loaded into the first unit to translate the certain Java bytecodes.

250. The system of claim 249 wherein the first unit and the hardware unit are part of a central processing unit.

251. The system of claim 249 wherein the first unit comprises a central processing unit and the hardware unit is outside the central processing unit.

252. The system of claim 249 wherein the certain bytecodes that are not translated in the hardware unit include method invocations.

253. The system of claim 249 wherein the first unit includes a register file and wherein a portion of the Java operand stack is stored in the register file.

254. A system comprising:

a first unit adapted to execute stack-based instructions; the first unit including a register file adapted to be manipulated using register-based instructions, the register file adapted to store a portion of an operand stack; and

a hardware unit adapted to convert stack-based instructions into register-based instructions, wherein the hardware unit is adapted to use the portion of the stack stored in the register file in order to convert more than one stack-based instructions into fewer register-based instructions.

255. The system of claim 254 in which the first unit and hardware unit are part of a central processing unit.

256. The system of claim 254 wherein the first unit comprises a central processing unit and the hardware unit is outside the central processing unit.

257. The system of claim 254 wherein multiple stack-based instructions pass through the hardware unit concurrently throughout the operation of combining logic.

258. The system of claim 254 wherein the hardware unit is adapted to convert a basic operand instruction and one or more stack manipulation instructions into a single register-based instruction.

259. The system of claim 254 wherein one of the multiple stack-based instructions includes a load or store instruction.

260. The system of claim 254 wherein the hardware unit includes an indication of the depth of the portion of the operand stack stored in the register file.

261. The system of claim 254 wherein the hardware unit includes an indication of the depth of the portion of the operand stack stored in the register file.

262. The system of claim 254 wherein the hardware unit includes logic to keep track of how many entries have been placed on the operand stack.

263. The system of claim 254 wherein the hardware unit keeps track of a top-of-stack register location, wherein the top-of-stack register in the first unit's register file is not fixed and can change as a result of an executed instruction.

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264. The system of claim 254 wherein the hardware unit keeps track of which registers in the first unit's register file contain portions of the Java operand stack, the meaning of the registers being able to change as a result of an executed instruction.

265. The system of claim 254 wherein the stack-based instructions are Java bytecodes.

266. A system comprising:

a first unit adapted to execute register-based instructions, the first unit having two sets of register files; and

a hardware unit associated with the first unit, the hardware unit adapted to convert stack-based instructions into register-based instructions, wherein one set of register files are used by the first unit when converted instructions are provided by the hardware unit.

267. The system of claim 266 wherein the first unit and the second unit are part of a central processing unit.

268. The system of claim 266 in which the first unit comprises a central processing unit and the hardware unit is not part of the central processing unit.

269. The system of claim 266 wherein the stack-based instructions are Java bytecodes.

270. The system of claim 266 wherein the hardware unit is adapted to examine stack-based instructions to determine whether multiple stack-based instructions can be combined into fewer register-based instructions.

271. The system of claim 266 in which the hardware unit produces register-based instructions that access a portion of the operand stack in the register file so as to reduce the number of register-based instructions that would otherwise be required.

272. The system of claim 266 wherein the other set of register files is used by the first unit when the hardware unit is bypassed.

273. The system of claim 272 in which a multiplexer is used to bypass the hardware unit when the other set of register files is used.

274. The system of claim 266 in which the hardware unit produces an indication sent to the first unit so that the first unit can determine which set of register files is to be used.

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275. The system of claim 266 in which the hardware unit includes an indication of the depth of the portion of the operand stack stored in the register file.

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